EPT9542 Product Brief

EPT9542 is a TFT LCD timing controller with 6/8-bit LVDS receiver and 1/2 port, 3/6 pairs, 6/8-bit Mini-LVDS transmitter. The Mini-LVDS is a low voltage swing interface for low power consumption and maximum clock up to 560MHz. The timing controller can output the control timing to source and gate drivers. It supports up to 1920x1200 resolution.

Features

- General
  - Support 1920x1200 FHD TFT-LCD Panel
  - Support 100Hz at Max. 1920x1200
  - Support 120Hz at Max. 1920x1080
  - Support DE-only Mode
  - Support I^{2}C Master controller (330KHz, variation: -20%, +19%)
  - Support Pattern Detect Function (PDF)
  - Support I^{2}C Master Controller for 16/32Kbit EEPROM download（selection by different package）
  - Built-in Oscillator (84MHz)
  - Supply Voltage 3.3V/2.5V/1.1V and built-in Low Voltage Reset (LVR)
- Input
  - 1/2 Port 6/8bit LVDS Receiver, clock frequency from 40MHz to 145MHz
  - Support JEIDA and NS LVDS format mapping
  - Support Input Spread Spectrum LVDS Signal
  - Support port swap and PN swap function
  - Support mirror function
  - Built-in termination resistors
  - Built-in pull-down resistors for clock pairs
- Output
  - Support Mini-LVDS interface
  - Mini-LVDS Transmitter
    - ✓ Support maximum bit rate from 120MHz to 560MHz
    - ✓ Support 2 port, 3 pair, 6/8bit @ LVDS 1 Port / 2 Port
    - ✓ Support 1 port, 6 pair, 6/8bit @ LVDS 1 Port / 2 Port
    - ✓ Support 1 port, 3 pair, 6/8bit @ LVDS 1 Port
    - ✓ Support two set of offset voltage
      - ■ Case1) 0.35V ~ 0.75V, step 50mV
      - ■ Case2) 0.5V ~ 1.2V, step 50mV
  - Support clock to data and clock to clock skew control
  - EMI solution
    - ✓ Built-in Spread spectrum clock generator
    - ✓ Built-in Slew rate control

- ✓ Adjustable output swing
  - Support Port swap and P/N swap
- Testability
  - Support general BIST Function
  - Support Samsung BIST spec
  - Support Fail-Safe Mode
- Image Enhancement
  - Support Gamma correction function
  - Support Dithering (FRC) function
  - Support Pattern Detect function
- LCD Driving
  - Support GOA (GOP) timing
  - Support max. 8 GOA clock
  - Support Dual Gate Data mapping
  - Support various pixel cell mapping
  - Support Reverse Scan
- Packaging
  - 64pin TQFP with ePAD (7mm x 7mm)