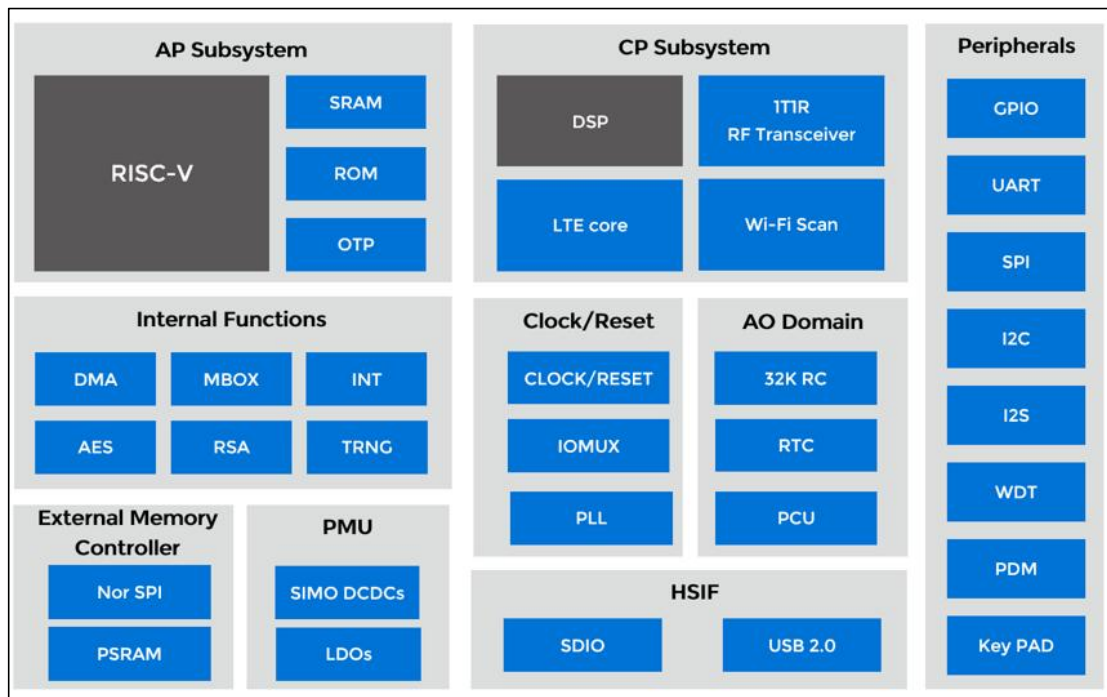


ECM9100-P is a highly integrated Open-CPU Cat.1bis SoC. It complies with the 3GPP Rel15 Cat.1bis standard and provides a competitive 4G digital module chip solution.

Block Diagram



Features

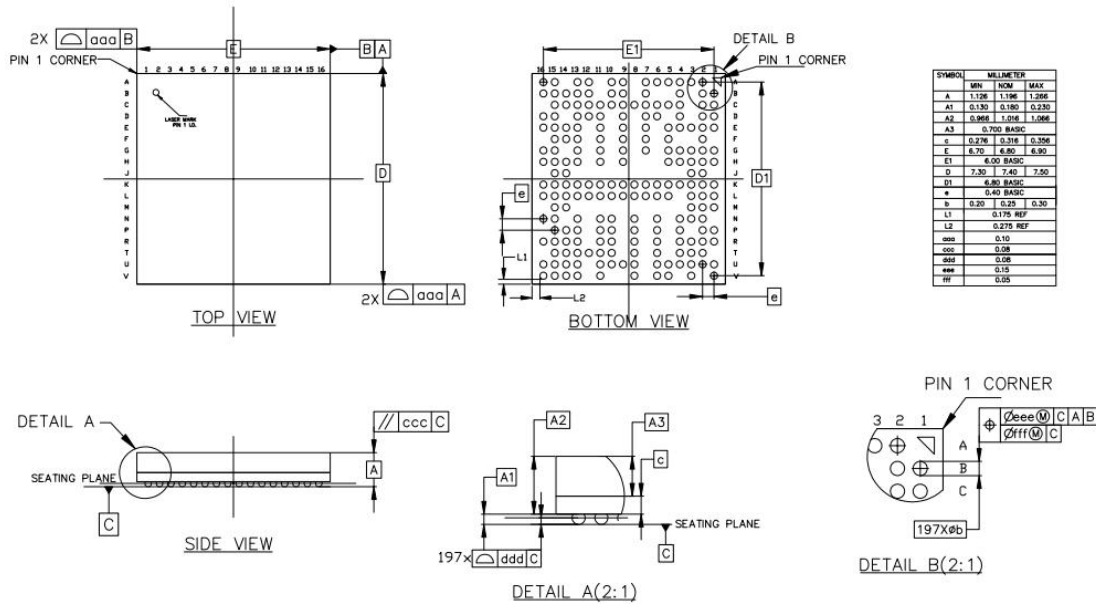
- Processor
 - AP processor uses a RISC-V processor with up to 491MHz and supports TCM and Cache
 - DSP Processor processes the Cat1 physical layer and protocol stack and supports TCM and Cache
- Memory
 - 4MB NOR Flash
 - 8MB PSRAM
 - 32KB SRAM, support Light sleep, Deep sleep, and Shut down modes
 - 1K Bits OTP
- Peripherals
 - 64 × GPIOs
 - 1 × USB2.0
 - 3 × UARTs. UART0 supports flow control, and the interface rate can reach 3Mbps
 - 3 × SPIs
 - 3 × I²C
 - 2 × I²S
 - 1 × SDIO3.0

- 4 × ADC
- 6 × PWM
- Keypad: 6 x 6
- 2 × PDM, supporting digital voice playback
- Support 0.3M@SPI, QVGA
- RF
 - FDD/TDD
 - 3GPP R15 Cat.1& Cat.1bis
 - FDD: B1/2/3/4/5/7/8/13/14/19/20/25/26/28/66/71
 - TDD: B34/38/39/40/41
 - Support BW: 1.4/3/5/10/15/20MHz
 - The maximum rate can reach 10Mbps (DL)/5Mbps (UL)
 - Support CAT1 RF transceiver
 - Support low-power consumption
 - RX supports high dynamic range
 - Support low phase noise Frac-N frequency synthesizers
 - Support direct transformation architecture
 - Low EVM
 - Support LDO
- Baseband
 - 3GPP Rel15 Cat.1bis
 - Maximum rate can be up to DL 10Mbps/UL 5Mbps
 - TDD/FDD
 - Supported bands: 1.4/3/5/10/15/20MHz
 - -98dBm Sensitivity @10M BW
 - 1.5mA @DRX 1.28s sleep mode
- Security
 - Secure boot
 - AES, RSA, and TRNG
- Voltage
 - Single power supply
 - Voltage range 2.8~5.5V
 - Interface voltage ranges from 1.8 to 3.3V, which can be configurable through the software
- Power Consumption
 - PSM 7μA
 - DRX@1.28s: 1.8mA
 - Support Light sleep/Deep sleep

Packaging and Order Information

Dimension

ECM9100-P uses FCCSP packaging with 195 pins. The size is 6.8mm × 7.4mm.



Order Information

Product No.	Packaging	Operating Temperature
ECM9100-P	FCCSP BGA195	-40~+85°C

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