Certificate

No.: 968/FSP 3105.00/26

Product tested	Soft Intellectual Property (IP) RISC-V processor	**Certificate holder**	Beijing ESWIN Computing Technology Co., Ltd. Room 101, 1st Floor, Building 3, No.18, Kechuang 10th Street, BDA (Beijing Economic Technological Development Area), Beijing City, P.R China
Type designation	R520A For details see actual “Revision List”		
Codes and standards	ISO 26262-2:2018 ISO 26262-5:2018		ISO 26262-8:2018 ISO 26262-9:2018
Intended application	The soft Intellectual Property (IP) RISC-V processor R520A, developed as a Safety Element out of Context (SEooC), complies with the requirements of ISO 26262 for ASIL D regarding the avoidance of systematic faults. Based on an exemplary configuration, ESWIN showed that the target values for the random hardware fault metrics according to ISO 26262-5, Clause 8 and 9 for ASIL D can be fulfilled. It can be used in applications, in order to realize safety goals, up to ASIL D according to ISO 26262. In addition to the above listed standards ISO 26262-10 and ISO 26262-11 were used to support the assessment.		
Specific requirements	The integrator/user is obliged to validate the assumptions and constraints defined by the manufacturer, under consideration of the instructions of safety manual, user manual and integration manual.		

Valid until 2031-02-11

The issue of this certificate is based upon an evaluation in accordance with the Certification Program CERT FSP2 V3.0:2020 in its actual version, whose results are documented in Report No. 968/FSP 3105.00/26 dated 2026-02-09. This certificate is valid only for products, which are identical with the product tested. Issued by the certification body accredited by DAkkS according to DIN EN ISO/IEC 17065. The accreditation is only valid for the scope listed in the annex to the accreditation certificate D-ZE-11052-02-00.

Köln, 2026-02-11

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Certification Body Safety & Security for Automation & Grid

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